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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,003	PADHI ET AL.	
	Examiner	Art Unit	
	Edna Wong	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :November 3, 2003 and January 16, 2004.

Election/Restrictions

Applicant's election without traverse of Group **I**, claims **1-19**, in the reply filed on August 9, 2007 is acknowledged.

The requirement is still deemed proper and is therefore made FINAL.

Specification

The disclosure is objected to because of the following informalities:

page 11, line 4, reference character "303" has been used to designate both the frame member and the frame portion (from page 10, line 25). It is unclear what reference character "303" designates.

page 19, line 30, the US patent application serial no. is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

I. Claims **5 and 9-19** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5

lines 1-2, "wherein palladium in the alloy is between *about 0.2 weight percent*

and ..." does not further limit wherein the alloy comprises *about 1.5 weight percent* of palladium" as recited in parent claim 4, line 2.

Claim 9

line 4, it appears that "a substrate" is the same as the semiconductor substrate recited in claim 9, lines 1-2. However, it is unclear if it is.

Claim 13

line 2, "$PdSO_4$ and $PdCl_2$" are not palladium *ions*.

Claim 16

line 2, "wherein palladium in the alloy is between *about 0.2 weight percent* and ..." does not further limit wherein the alloy comprises *about 1.5 weight percent* of palladium" as recited in parent claim 15, line 2.

II. Claims **1-19** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: using the plating solution in the supplying step.

There is no relationship recited between the plating solution and the supplying step.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-3** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over **Kitaev et al.** (US Patent No. 6,174,812 B1).

Kitaev teaches a method for plating a homogenous copper-palladium alloy, comprising:

(a) providing a plating solution to an electrochemical plating cell (col. 14, Example 9), wherein the plating solution includes a copper ion source at a concentration of between about 0.1 M and about 1.0 M (= 0.0005-0.5 M/l $CuCl_2$) and a palladium ion source at a concentration of between about 0.0005 M and about 0.1 M (= 0.0005-0.5 M/l $PdCl_2$) [col. 6, lines 1-5]; and

(b) supplying an electrical deposition bias (= 4.8 V) to a plating surface (= a multilayer structure) [col. 14, Example 9], wherein the electrical deposition bias is

configured to simultaneously deposit copper ions and palladium ions onto the plating surface (*inherent*).

The concentration of the copper ion source is between about 0.4 M and about 0.8 M (= 0.0005-0.5 M/l $CuCl_2$) [col. 6, lines 1-5].

The palladium ion source comprises at least one of $PdSO_4$ and $PdCl_2$ (= 0.0005-0.5 M/l $PdCl_2$) [col. 6, lines 1-5].

The method further comprises annealing the alloy at a temperature of between about 200°C and about 400°C (= the continuous electrically conductive film from the end surfaces of metal layers the structure is preferably heat treated at 35°-400°C) [col. 3, lines 35-40].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

I. Claims **4-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kitaev et al.** (US Patent No. 6,174,812 B1) as applied to claims 1-3 above.

Kitaev is as applied above and incorporated herein.

The method of Kitaev differs from the instant invention because Kitaev does not disclose the following:

a. Wherein alloy comprises about 1.5 weight percent of palladium and about 98.5 weight percent of copper, as recited in claim 4.

b. Wherein the palladium in the alloy is between about 0.2 weight percent and about 1.5 weight percent, as recited in claim 5.

Kitaev teaches that the multilayer structure described in Example 1 was placed into the solution for deposition of a continuous electrically conductive palladium film as described in Example 1 between two gold-plated reticular copper electrodes of a size of 200x300 mm extending in parallel therebetween and connected to an AC power supply source (col. 9, Example 1; and col. 14, Example 9).

The invention as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made because Kitaev teaches a similar plating method as presently claimed. Similar processes can reasonably be expected to yield products which inherently have the same properties. *In re Spada* 15 USPQ 2d 1655 (CAFC 1990); *In re DeBlauwe* 222 USPQ 191; *In re Wiegand* 86 USPQ 155 (CCPA 195).

c. Wherein the annealing is for a duration of between about 30 seconds and about 60 minutes, as recited in claim 6.

Kitaev teaches heat treating the continuous electrically conductive film at 35°-400°C (col. 3, lines 35-40). The heat treating inherently has a duration.

Kitaev also teaches that the temperature and the exposure time depend upon the

properties of the film **6** and the material of the dielectric layers **2** (col. 8, lines 25-27).

Kitaev also teaches that in some cases the structure having the auxiliary electrically conductive film applied thereto is subjected to a heat treatment at 35°-400°C for 10-90 minutes (col. 9, lines 5-7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the heat treating described by Kitaev with wherein the annealing is for a duration of between about 30 seconds and about 60 minutes because the duration is a result-effective variable and one skilled in the art has the skill to calculate the duration that would have determined the success of the desired reaction to occur, e.g., depending upon the properties of the film and the material of the dielectric layers (MPEP § 2141.03 and § 2144.05(II)(B)).

d. Wherein the electrical deposition bias has a current density of between about 0.5 mA/cm^2 and about 80 mA/cm^2 over the plating surface, as recited in claim 7.

Kitaev teaches an alternating current of 4.5 A was applied to the independent electrodes at 4.8 V. This treatment resulted in uniform formation of a continuous electrically conductive palladium on the hole walls of thickness of 200 nm in 3.5 minutes (col. 14, Example 14).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the electrical deposition bias described by Kitaev with wherein the electrical deposition bias has a current density of between about 0.5

mA/cm^2 and about 80 mA/cm^2 over the plating surface because the electrical deposition bias is a result-effective variable and one skilled in the art has the skill to calculate electrical deposition bias that would have determined the success of the desired reaction to occur, e.g., resulting in uniform formation of a continuous electrically conductive palladium on the hole walls of thickness of 200 nm in 3.5 minutes (MPEP § 2141.03 and § 2144.05(II)(B)).

II. Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kitaev et al.** (US Patent No. 6,174,812 B1) as applied to claims 1-3 above, and further in view of **Ritter et al.** (US Patent Application Publication No. 2007/0014075 A1).

Kitaev is as applied above and incorporated herein.

The method of Kitaev differs from the instant invention because Kitaev does not disclose wherein the method further comprises rotating the plating surface between about 5 RPM and about 60 RPM while the electrical deposition bias is supplied to the plating surface, as recited in claim 8.

Kitaev teaches that in a number of examples the multilayer structure is referred to as a printed circuit board as the most typical example of multilayer structures consisting of alternating dielectric and metal layers (col. 9, lines 20-25).

Like Kitaev, Ritter teaches electroplating end faces of structural layers (page 1, [0002]). Ritter teaches that a plurality of electronic components is barrel plated in a 2.5x4 inch barrel at 16 rpm for about 60 minutes (page 10, [0119]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Kitaev with wherein the method further comprises rotating the plating surface between about 5 RPM and about 60 RPM while the electrical deposition bias is supplied to the plating surface because this would have barrel plated a plurality of electronic components as taught by Ritter (page 10, [0119]).

The reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by the Applicants. *In re Linter* 458 F.2d 1013, 173 USPQ 560 (CCPA 1972); *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990), *cert. denied*, 500 US 904 (1991); and MPEP § 2144.

III. Claims **9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hsiung et al.** (US Patent No. 6,174,812 B1).

Hsiung teaches a method for electrochemically plating an alloy onto a semiconductor substrate (= the ULSI circuit fabrication) [col. 1, lines 6-9], comprising:

(a) providing a plating solution containing copper ions and palladium ions (= from electroplating a copper-palladium alloy gap-fill electroplating layer **23**) [col. 2, lines 50-53];

(b) immersing a working surface of a substrate **20** (= an oxide layer gap

substrate) [col. 2, lines 46-48] and an anode in the plating solution (= from electroplating a copper-palladium alloy gap-fill electroplating layer **23**) [col. 2, lines 50-53]; and

(c) applying an electrical plating bias between the anode and the working surface (= from electroplating a copper-palladium alloy gap-fill electroplating layer **23**) [col. 2, lines 50-53], wherein the electrical plating bias is configured to simultaneously plate copper and palladium out of the plating solution and onto the working surface (= ECD technology allows Cu-Pd being codeposited on the copper seed layer with underlying TaN barrier) [col. 3, lines 63-65].

The electrical plating bias comprises a constant electrical bias (= from electroplating a copper-palladium alloy gap-fill electroplating layer **23**) [col. 2, lines 50-53].

The method further comprises annealing the alloy at a temperature (= next, a copper-palladium is carried out through an annealing process) [col. 2, lines 55-56].

IV. Claim **11** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hsiung et al.** (US Patent No. 6,174,812 B1) as applied to claims 9 and 10 above, and further in view of **Moiseeva et al.** ("Palladium-Copper Alloy Electrodeposition with a Pulsed Current", *Intensifik. Tekhnol. Protsessov pri Gsazhdenil Met. I Splavov* (1997), pp. 92-93, From: Ref. Zh. Metall, 1978, Abstr. No. 2G293) and **Van Horn** ("Pulse Plating", *Dynatronix* (August 5, 1999), pp. 1-13).

Hsiung is as applied above and incorporated herein.

The method of Hsiung differs from the instant invention because Hsiung does not disclose wherein the electrical plating bias comprises a pulsed bias, wherein a first portion of the pulse is configured to primarily plate copper and a second portion of the pulse is configured to primarily plate palladium, as recited in claim 11.

Like Hsiung, Moiseeva teaches electrochemically plating a palladium-copper alloy (abstract). Moiseeva teaches electrochemically plating the palladium-copper alloy with a pulse current (abstract).

Van Horn teaches that the advantages of pulse plating most common are producing fine-grained deposits, reducing the variation in thickness from one part to the next, increasing plating speeds, and reducing the need for organic additives (page 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the electrical plating bias described by Hsiung with wherein the electrical plating bias comprises a pulsed bias, wherein a first portion of the pulse is configured to primarily plate copper and a second portion of the pulse is configured to primarily plate palladium because electrochemically plating the palladium-copper alloy with a pulse current would have had advantages such as producing fine-grained deposits, reducing the variation in thickness from one part to the next, increasing plating speeds, and reducing the need for organic additives as taught by Van Horn (page 1).

The reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not

necessary that the prior art suggest the combination to achieve the same advantage or result discovered by the Applicants. *In re Linter* 458 F.2d 1013, 173 USPQ 560 (CCPA 1972); *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990), *cert. denied*, 500 US 904 (1991); and MPEP § 2144.

Furthermore, when electrochemically depositing two different metals having different deposition potentials from an electroplating solution, the metal having the lower magnitude deposition potential will generally plate out from the solution first.

V. Claims **12-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hsiung et al.** (US Patent No. 6,174,812 B1) as applied to claims 9 and 10 above, and further in view of **Kitaev et al.** (US Patent No. 6,174,812 B1).

Hsiung is as applied above and incorporated herein.

The method of Hsiung differs from the instant invention because Hsiung does not disclose the following:

a. Wherein the amount of copper ions in the plating solution is between about 0.1 M and about 1.0 M and the amount of palladium ions in the plating solution is between about 0.0005 M and about 0.1 M, as recited in claim 12.

b. Wherein the palladium ions comprise at least one of $PdSO_4$ and $PdCl_2$, as recited in claim 13.

c. Wherein the amount of copper ions in the plating solution is between about 0.4 M and about 0.8 M, as recited in claim 14.

Hsiung teaches electroplating a copper-palladium alloy.

Like Hsiung, Kitaev teaches electroplating a continuous film of metals in a solution containing: 0.0005-0.5 M/l $PdCl_2$, 0.0005-0.5 M/l $CuCl_2$ and 0.001-1M/l H_2SO_4 (col. 5, line 59 to col. 6, line 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the amount of copper ions, the amount of palladium ions, and the palladium ions described by Hsiung with wherein the amount of copper ions in the plating solution is between about 0.1 M and about 1.0 M and the amount of palladium ions in the plating solution is between about 0.0005 M and about 0.1 M; wherein the palladium ions comprise at least one of $PdSO_4$ and $PdCl_2$; and wherein the amount of copper ions in the plating solution is between about 0.4 M and about 0.8 M because such a solution would have deposited a copper-palladium alloy. It has been held that the selection of a known material based on its suitability for its intended use supports a prima facie obviousness determination (MPEP § 2144.06 and § 2144.07).

Furthermore, if the composition is physically the same, it must have the same properties. Products of identical chemical composition can not have mutually exclusive properties. A chemical composition and its properties are in separable (MPEP § 2112.01(II)).

d. Wherein the method further comprises plating the alloy onto the working

surface, wherein the alloy comprises about 1.5 weight percent of palladium and about 98.5 weight percent of copper, as recited in claim 15.

e. Wherein the palladium in the alloy is between about 0.2 weight percent and about 1.5 weight percent, as recited in claim 16.

Kitaev teaches that the multilayer structure described in Example 1 was placed into the solution for deposition of a continuous electrically conductive palladium film as described in Example 1 between two gold-plated reticular copper electrodes of a size of 200x300 mm extending in parallel therebetween and connected to an AC power supply source (col. 9, Example 1; and col. 14, Example 9).

The invention as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made because Kitaev teaches a similar plating method as presently claimed. Similar processes can reasonably be expected to yield products which inherently have the same properties. *In re Spada* 15 USPQ 2d 1655 (CAFC 1990); *In re DeBlauwe* 222 USPQ 191; *In re Wiegand* 86 USPQ 155 (CCPA 195).

VI. Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hsiung et al.** (US Patent No. 6,174,812 B1) as applied to claims 9 and 10 above, and further in view of **Kitaev et al.** (US Patent No. 6,174,812 B1) as applied to claims 12-16 above, and further in view of **Krishnamoorthy et al.** (US Patent No. 6,319,387 B1).

Hsiung and Kitaev are as applied above and incorporated herein.

The method of Hsiung differs from the instant invention because Hsiung does not disclose wherein annealing the alloy is at a temperature of between about 200°C and about 400°C for a duration of between about 30 seconds and about 60 minutes, as recited in claim 17.

Hsiung teaches that the copper-palladium is carried out through an annealing process (col. 2, lines 55-56). The annealing inherently has a temperature.

Like Hsiung, Krishnamoorthy teaches electroplating a copper-Me alloy. Krishnamoorthy teaches that annealing generally improved the resistivity of the copper-alloy layer when compared to the resistivity of the layer as originally deposited. The resistivity was not significantly enhanced with increasing annealing temperatures above about 350°C-400°C (col. 6, lines 7-26).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the annealing described by Hsiung with wherein annealing the alloy is at a temperature of between about 200°C and about 400°C because annealing would have generally improved the resistivity of the copper-alloy layer when compared to the resistivity of the layer as originally deposited as taught by Krishnamoorthy (col. 6, lines 7-26).

As for a duration of between about 30 seconds and about 60 minutes, the duration is a result-effective variable and one skilled in the art has the skill to calculate the duration that would have determined the success of the desired reaction to occur (MPEP § 2141.03 and § 2144.05(II)(B)).

VII. Claims **18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hsiung et al.** (US Patent No. 6,174,812 B1) as applied to claims 9 and 10 above, and further in view of **Krishnamoorthy et al.** (US Patent No. 6,319,387 B1).

Hsiung is as applied above and incorporated herein.

The method of Hsiung differs from the instant invention because Hsiung does not disclose the following:

a. Wherein the electrical plating bias has a current density of between about 0.5 mA/cm^2 and about 80 mA/cm^2 over the working surface, as recited in claim 18.

Hsiung teaches electroplating a copper-palladium alloy. The electroplating inherently has an electrical plating bias.

Like Hsiung, Krishnamoorthy teaches electroplating a copper-Me alloy. Krishnamoorthy teaches that when an attempt is made to electrochemically deposit two different metals having different deposition potentials from an electroplating solution, the metal having the lower magnitude deposition potential will generally plate out from the solution and a significant amount of gas will evolve before reaching the greater magnitude deposition potential of the other metal (col. 6, lines 38-58).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the electrical plating bias described by Hsiung with wherein the electrical plating bias has a current density of between about 0.5 mA/cm^2 and about 80 mA/cm^2 over the working surface because the electrical plating bias would have determined which metal will generally plate out from the solution as

taught by Krishnamoorthy (col. 6, lines 38-58).

b. Wherein the method further comprises rotating the substrate between about 5 RPM and about 60 RPM while applying the electrical plating bias between the anode and the working surface, as recited in claim 19.

Krishnamoorthy teaches that rotating the workpiece during the electrochemical deposition process enhances the uniformity of the resulting film (col. 9, lines 22-33).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Hsiung by rotating the substrate while applying the electrical plating bias between the anode and the working surface because rotating the workpiece during the electrochemical deposition process would have enhanced the uniformity of the resulting film as taught by Krishnamoorthy (col. 9, lines 22-33).

As to rotating the substrate between about 5 RPM and about 60 RPM, the duration is a result-effective variable and one skilled in the art has the skill to calculate the duration that would have determined the success of the desired reaction to occur (MPEP § 2141.03 and § 2144.05(II)(B)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edna Wong whose telephone number is (571) 272-1349. The examiner can normally be reached on Mon-Fri 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Edna Wong
Primary Examiner
Art Unit 1753

EW
August 23, 2007